

Application No. 09/440,928

Attorney Docket 040301-0578

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Nobutoshi AOKI et al.

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING INSULATED
GATE FIELD EFFECT TRANSISTOR AND METHOD OF
MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: 11/16/1999

Examiner: S. Rao

Art Unit: 2814

AMENDMENT TRANSMITTAL

Mail Stop Fee Amendment
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Transmitted herewith is an Amendment and Reply in the above-identified application.

- ☐ Small Entity status under 37 C.F.R. § 1.9 and § 1.27 has been established by a Small Entity statement previously submitted.
- ☐ Small Entity statement is enclosed.
- ☒ The fee required for additional claims is calculated below:

	Claims as Amended	Previously Paid For	Extra Claims Present	Rate	Additional Claims Fee
Total Claims:	30	28	2	x \$18.00	\$36.00
Independents:	10	8	2	x \$84.00	\$168.00
First presentation of any Multiple Dependent Claims:			+	\$280.00	\$0.00
CLAIMS FEE TOTAL:					\$204.00

- ☐ Applicant hereby petitions for an extension of time under 37 C.F.R. §1.136(a) for the total number of months checked below:

<input type="checkbox"/>	Extension for response filed within the first month:	\$110.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the second month:	\$410.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the third month:	\$930.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the fourth month:	\$1,450.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the fifth month:	\$1,970.00	\$0.00
	EXTENSION FEE TOTAL:		\$0.00
<input type="checkbox"/>	Statutory Disclaimer Fee under 37 C.F.R. 1.20(d):	\$110.00	\$0.00
	CLAIMS, EXTENSION AND DISCLAIMER FEE TOTAL:		\$204.00
<input type="checkbox"/>	Small Entity Fees Apply (subtract ½ of above):		\$0.00
	TOTAL FEE:		\$204.00

- ☐ Please charge Deposit Account No. 19-0741 in the amount of \$204.00. A duplicate copy of this transmittal is enclosed.
- ☒ A check in the amount of \$204.00 for additional claims fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date May 27, 2003
(Tuesday after holiday)

FOLEY & LARDNER
Customer Number: 22428



22428

PATENT TRADEMARK OFFICE

Telephone: (202) 672-5414
Facsimile: (202) 672-5399

By Aaron C. Chatterjee

Richard L. Schwaab
Attorney for Applicant
Registration No. 25,479

Aaron C. Chatterjee
Registration No. 41,398



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

17/F
6-6-03
J. Carter

Applicant: Nobutoshi AOKI et al.
Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING
INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD
OF MANUFACTURING THE SAME
Appl. No.: 09/440,928
Filing Date: November 16, 1999
Examiner: S. Rao
Art Unit: 2814

RECEIVED
MAY 30 2003
TECHNOLOGY CENTER 2800

AMENDMENT AND REPLY UNDER 37 C.F.R. § 1.111

Mail Stop FEE AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In reply to the Office Action mailed February 25, 2003, please amend the above-identified application as follows:

IN THE DRAWINGS:

FIG. 3 has been amended as shown in red on the drawings attached to the Proposed Changes to the Drawings, being filed concurrently herewith.

IN THE CLAIMS:

Please amend the claims by replacing the indicated claims with the following clean version. (See Attachment A for the marked up version of the amended claims.)

- FI
1. (Five Times Amended) A semiconductor device comprising:
a pair of main electrodes used as source and drain electrodes;
a channel forming region provided between the pair of main electrodes;
an insulating gate film formed on the channel forming region; and

05/29/2003 MBIZUNES 00000072 09440928

01 FC:1202
02 FC:1201

36.00 OP
168.00 OP